Research Publications (Dr. Sanjeev Rai)

SCI JOURNAL PUBLICATIONS

1.	Manish Kumar Rai, Abhinav, Sanjeev Rai, "Comparative Analysis & study of various Leakage Reduction Techniques for Short Channel devices in Junctionless Transistors: A Review and Perspective." Silicon (2021)
2.	Vidyadhar Gupta, Nitish Kumar, Himanshi Awasthi, Sanjeev Rai, Amit Kumar Pandey, Abhinav Gupta, "Temperature dependent analytical modeling of Graded-Channel Gate-All-Around (GC-GAA) Junctionless Field-Effect Transistors (JLFETs)" Journal of Electronic Materials, (2021) Springer.
3.	Amrish Kumar, Sanjeev Rai, "Compact Modeling and Analysis of Charge and Device Capacitance for SELBOX Junctionless Transistor." Silicon (2021).
4.	Kumar, Amrish, Yashu Swami, and Sanjeev Rai. "Modeling of surface potential and fringe capacitance of selective buried oxide junctionless transistor." *Silicon* (2020): 1-9.
5.	Swami, Yashu, and Sanjeev Rai. "Ultra-thin high-K dielectric profile based NBTI compact model for Nanoscale bulk MOSFET." *Silicon* 11, no. 3 (2019): 1661-1671.
6.	Yashu Swami and Sanjeev Rai. "Comprehending and Analyzing the Quasi-Ballistic Transport in ultra slim nano-MOSFET through Conventional Scattering Model", *Journal of Nanoelectronics and Optoelectronics* 2019 Jan 1; 14(1):80-91.
7.	Yashu Swami, Sanjeev Rai, "Modeling and Characterization of Inconsistent Behavior of Gate Leakage Current with Threshold Voltage for Nano MOSFETs", *American Journal of Modern Physics*. Vol. 7, No. 4, 2018, pp. 166-172. doi: 10.11648/j.ajmp.20180704.14
8.	Yashu Swami and Sanjeev Rai. "Ultra-Thin High-K Dielectric Profile based NBTI Compact Model for Nanoscale Bulk MOSFET", *Silicon* (2018): 1-11. https://doi.org/10.1007/s12633-018-9984-z
9.	Amrish Kumar, Abhinav Gupta, **Sanjeev Rai**, "Reduction of self-heating effect using selective buried oxide (SELBOX) charge plasma based junctionless transistor", AEU - International Journal of Electronics and Communications, vol. 95, pp. 162-169, 2018.
10.	Abhinav Gupta, Anamika Singh, S. K. Gupta, **Sanjeev Rai**, " Potential Modeling of Oxide Engineered Doping-Less Dual-Material-Double-Gate Si–Ge MOSFET and Its Application", Journal of nanoelectronics and optoelectronics, vol. 13, pp. 1115-1122, 2018.
11.	**Sanjeev Rai**, Abhinav, "Analytical modeling and analysis of spacer induced shallow source/drain extension junction-less double gate (SDE-JLDG) MOSFET incorporating fringing field effects", Journal of nanoelectronics and optoelectronics, vol. 13, pp. 168-177, 2018.
12.	**Sanjeev Rai**, Abhinav, "Reliability Analysis of Junction-less Double Gate (JLDG) MOSFET for Analog/RF Circuits for High Linearity Applications", *Microelectronics Journal* 64 (2017): 60-68. *MEJ 3878.* https://doi.org/10.1016/j.mejo.2017.04.009 impact factor 1.163, ISSN no. 0026-2692
13.	Swami, Yashu, and **Sanjeev Rai**. "Modeling and analysis of sub-surface leakage current in nano-MOSFET under cutoff regime"; Superlattices and Microstructures 102 (2017): 259-272. DOI: 10.1016/j.spmi.2016.12.044 impact factor 2.123, ISSN no. 0749-6036.
14.	Yashu Swami and Sanjeev Rai. "Modeling, Simulation, and Analysis of Novel Threshold Voltage Definition for Nano-MOSFET", *Journal of Nanotechnology* 2017 (2017). https://doi.org/10.1155/2017/4678571
15.	Nirmal Ch. Roy**,** Abhinav & **Sanjeev Rai,** Analytical Surface Potential Modeling and Simulation of Junction-less Double Gate (JLDG) MOSFET for Ultra low-power Analog/RF Circuits, *Microelectronics Journal, Vol-46*, **ISBN/ISSN No.** 0026-2692
16.	Manoj KumarYadav, Santosh KumarGupta, SanjeevRai, Avinash C.Pandey, Al embedded MgO barrier MTJ: A first principle study for application in fast and compact STT-MRAMs, Superlattices and Microstructures, Vol-103, **ISBN/ISSN No.** 0749-6036